AD-A152 120 DIGITAL RF DELAY LINE FOR ECM (ELECTRONIC COUNTERMEASURE) LOOK-THROUGH(U) RAYTHEON CO GOLETA CA ELECTROMAGNETIC SYSTEMS DIV 18 DEC 84 N00039-81-C-0361 1/1

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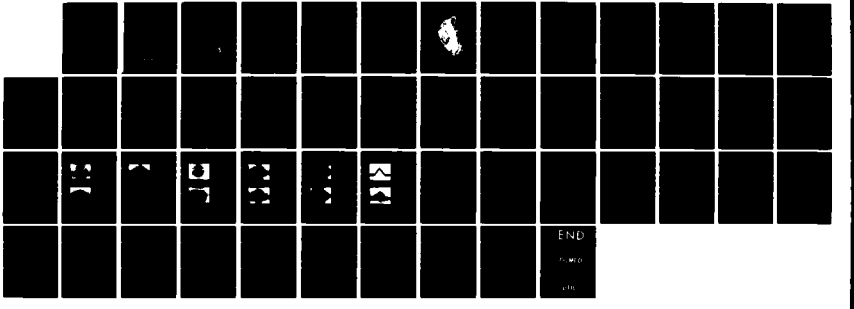
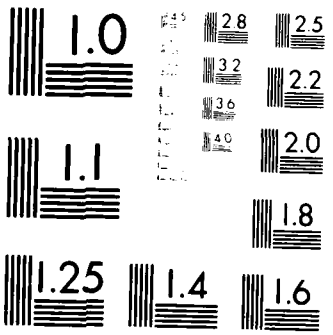


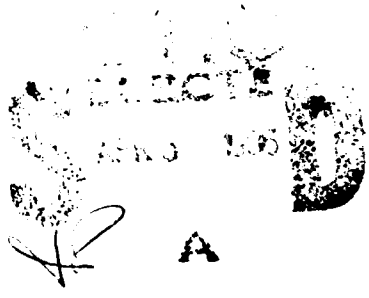


DIGITAL RF DELAY LINE FOR ECM LOOK-THROUGH

SUBMITTED TO
NAVAL ELECTRONICS SYSTEMS COMMAND
WASHINGTON, D.C. 20360

CONTRACT NO.
N00039-81-C-0361

18 DECEMBER 1984



RAYTHEON

RAYTHEON COMPANY
ELECTROMAGNETIC SYSTEMS DIVISION
6380 HOLLISTER AVENUE
GOLETA, CA 93117

DIGITAL RF DELAY LINE

FOR

ECM LOOK-THROUGH

Submitted to

Naval Electronics Systems Command
Washington, D.C. 20360

Contract N00039-81-C-0361

Submitted by

Raytheon Company
Electromagnetic Systems Division
6380 Hollister Ave.
Goleta, CA 93117

18 December 1984

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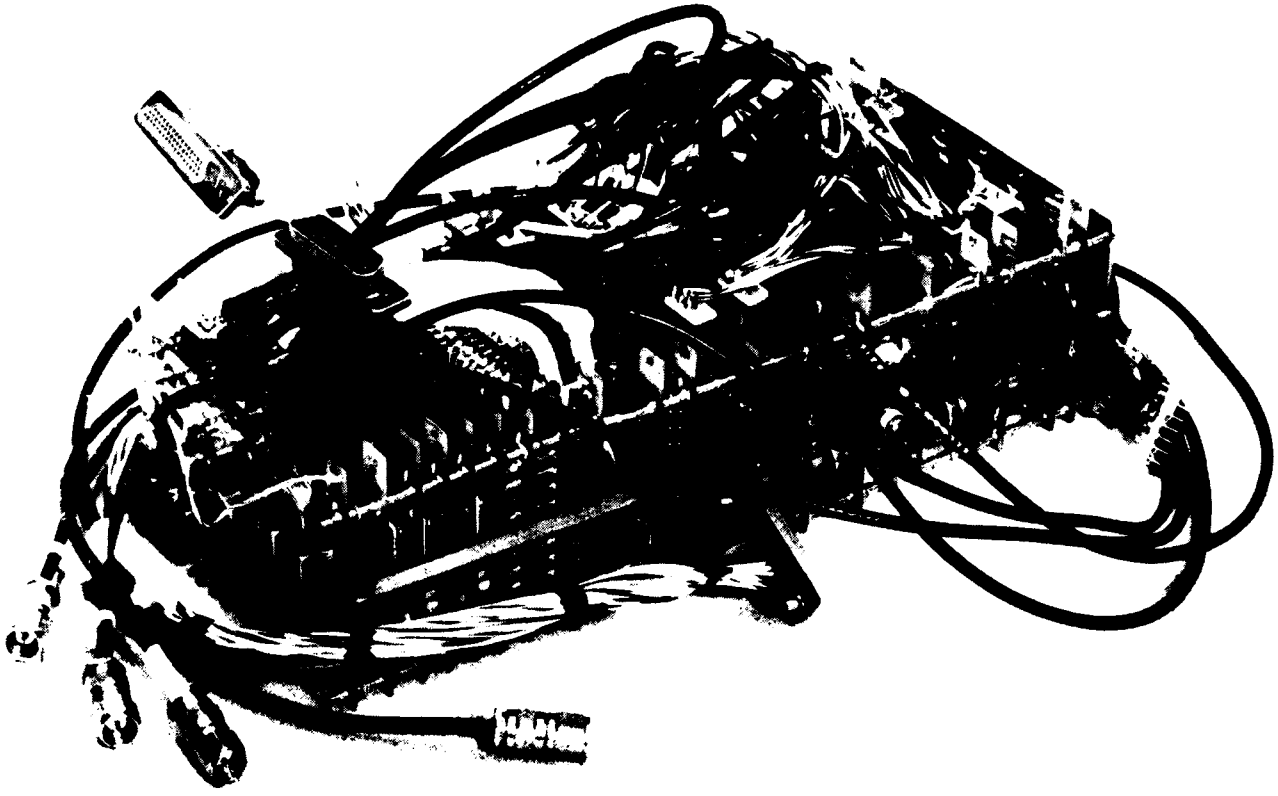
ABSTRACT

Jamming signals, when reflected from structure to receiver, produce unwanted reflected signal interference in a countermeasure system. Elimination of these reflections would increase look-through capability. It is the goal of this project to demonstrate Digital RF Memory (DRFM) techniques which would null these unwanted reflected signals.

Controlled injection of a transmitter signal into a receiver is a method of nulling this interference. Successfull nulling requires control of delay, phase, and gain of the feedback signal. The feasibility of using sampling electronics for storage and delay control was demonstrated in this project. The DRFM was used to simulate the electronic countermeasure (ECM) transmitter. Delays in the injection path were generated with high rate shift registers. The phase and gain of the injection paths were set with linear elements. The results from the experiment include bandwidth and quality of available nulls, as well as recommendations for the selection of nulling strategy.

RAYTHEON

THREE PORT DRFM



SECTION 1.
INTRODUCTION

A special DRFM was designed and tested. This unit had three coherent output ports. Figure 1 shows the actual unit (design details are provided in Appendix A). One port provided a reference signal, the other two provided digitally delayed copies of the same signal.

Experiments were run using the digitally delayed signals to null analog delayed copies of the reference signal.

Section 2 discusses the general nature of the multiple delayed interfering signals, the benefits of time delay match, and several strategies for alignment. Section 3 discusses the test setup, Section 4 outlines the test sequence, and Section 5 gives the test results. Appendix A describes the electrical and mechanical design of the DRFM. A companion paper describes the use of DRFM techniques in system ECM look-through applications.[1]

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[1] Final Report for Adaptive Cancellation Techniques, Contract N00014-81-C-20375, Submitted to the Naval Research Laboratory, Washington, D.C.

SECTION 2.
DISCUSSION OF THE PROBLEM

In a system that must simultaneously receive and transmit, signals from the transmitter find their way into the receiver and raise the receiver noise level. These signals may reflect from a nearby structure, or may couple directly by way of antenna sidelobes. Cancellation of either mode can be accomplished if the sample of the transmitted signal is coherent, or can be made coherent with the received signal. Presented in this section are time, frequency, and phase domain descriptions of the problem, as well as solutions.

A model of the reflected case is illustrated in Figure 1.

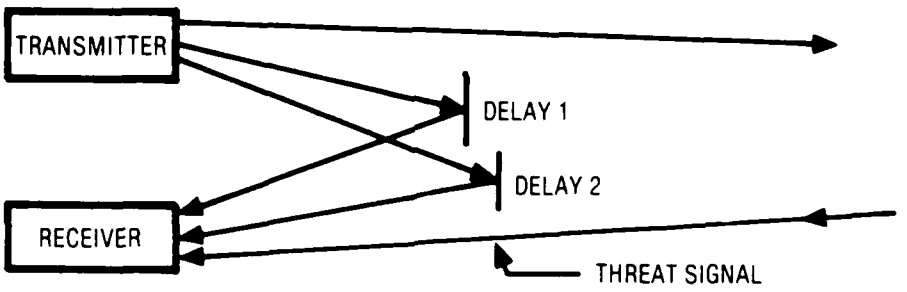


Figure 1. Reflected Case Model

A model of the reflection model may be simulated with delay lines as shown in Figure 2.

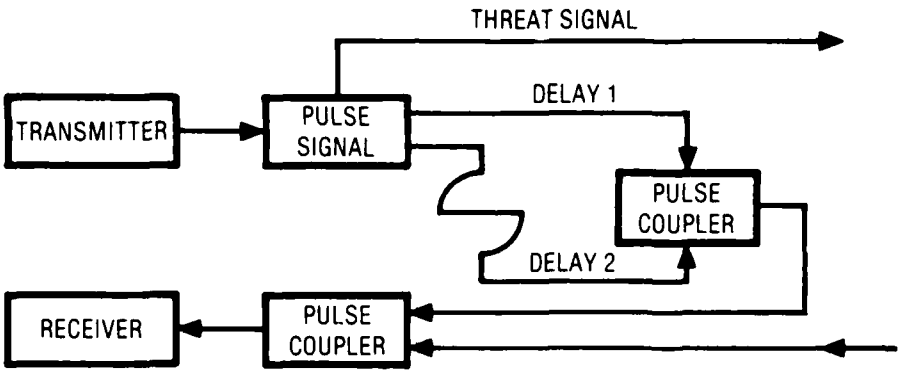


Figure 2. Reflection Case Model with Simulated Delay Lines

The delay 1 and 2 signals are summed with received signals to produce higher noise levels.

To null an interfering signal, the feedback signal must be controlled in phase (ϕ), gain (G) and delay (D). It is useful to discuss the problem in time, phase as a function of frequency, and amplitude as a function of frequency.

Signals, separated by a few nanoseconds, may arrive at the receiver to interfere with other incoming signals. This situation is illustrated in the time domain in Figure 3.

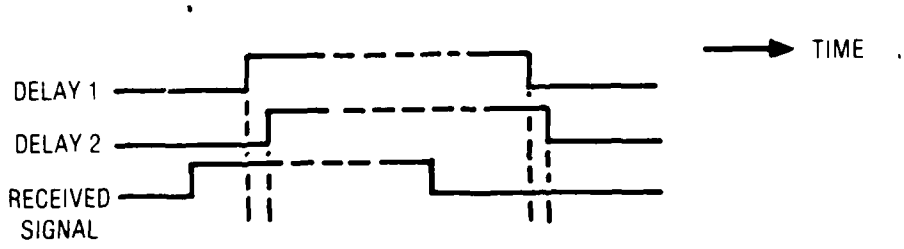


Figure 3. Separated Signals in the Time Domain

A delay line has phase as well as time characteristics. The phase characteristic of a delay line shows linearly increasing phase as a function of frequency. (See Figure 4.)

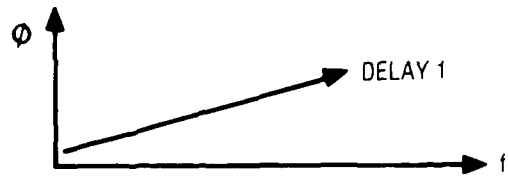


Figure 4. Delay Line Showing Linearly Increasing Phase

The scope of the phase/frequency characteristic is controlled by the length of the cables. Two cable characteristics are illustrated in Figure 5 as delay 1 and 2.

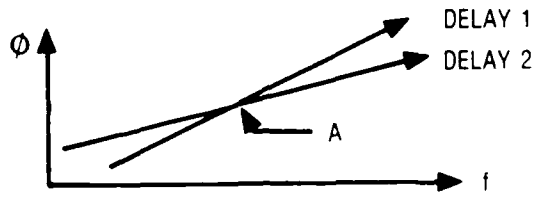


Figure 5. Illustrated Cable Characteristics (delay 1 and 2)

If the signals from delay 1 and 2 were subtracted, there would be a null at Point A (assuming the amplitude of A equals the amplitude of B).

In the frequency domain, the addition of the signals shown in Figure 5 would produce a multi-cusp amplitude frequency characteristic as shown in Figure 6.

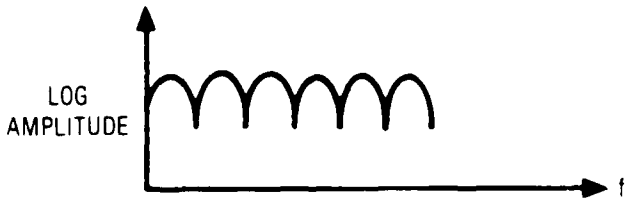


Figure 6. Multi-cusp Amplitude Frequency Characteristic

The cusps are formed at points when phase equals 2, 360, and 720 degrees. The distance between cusps increases as the differential length of the cables decreases. Cables of equal length produce no cusps.

There are two ways to null a single reflection. A delayed signal equal to the reflected signal in phase, gain, and delay will be called the 1-on-1 strategy. The 2-on-1 strategy is formed by setting the delays of two feedback channels unequal to the reflected signal. The phase and gain are set for maximum bandwidth null. The 2-on-1 strategy is the simplest case of N-on-1.

1-ON-1 NULL

If a single uncontrolled delay (reflected path) is matched with a path that is controlled in delay, phase, and amplitude, a broadband null may be formed. Figure 7 illustrates a block diagram of such a circuit.

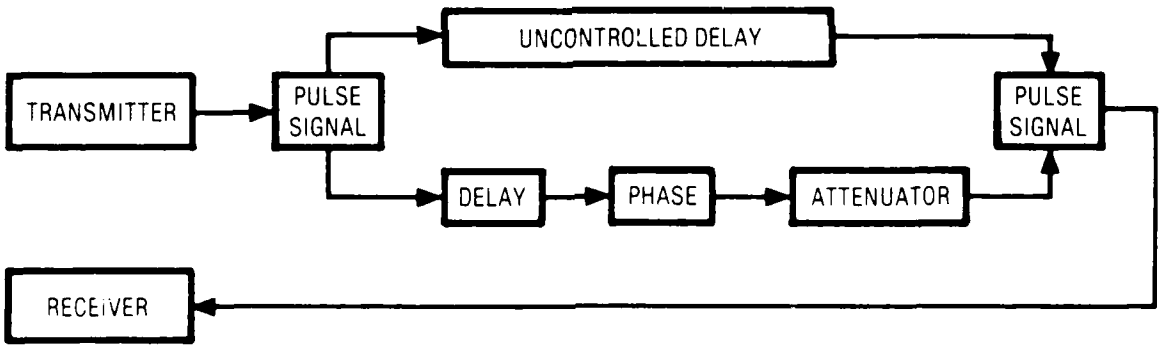


Figure 7. Block Diagram of 1-on-1 Null

If phase, gain, and delay can be matched between the two channels from f_o to f_1, a null will be formed. If phase or gain are not equal outside of f_o and f_1, the null quality suffers. Figure 8 shows the phase characteristic. Figure 9 shows the amplitude null characteristic.

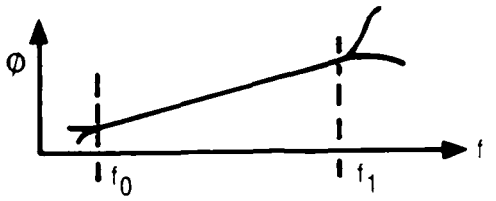


Figure 8. Phase Characteristic

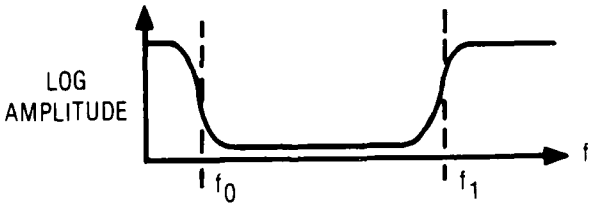


Figure 9. Amplitude Null Characteristic

2-ON-1 NULL

A 2-on-1 null is produced by combining two controlled phase/gain paths with a single uncontrolled delay (reflected path). A simplified block diagram is shown in Figure 10.

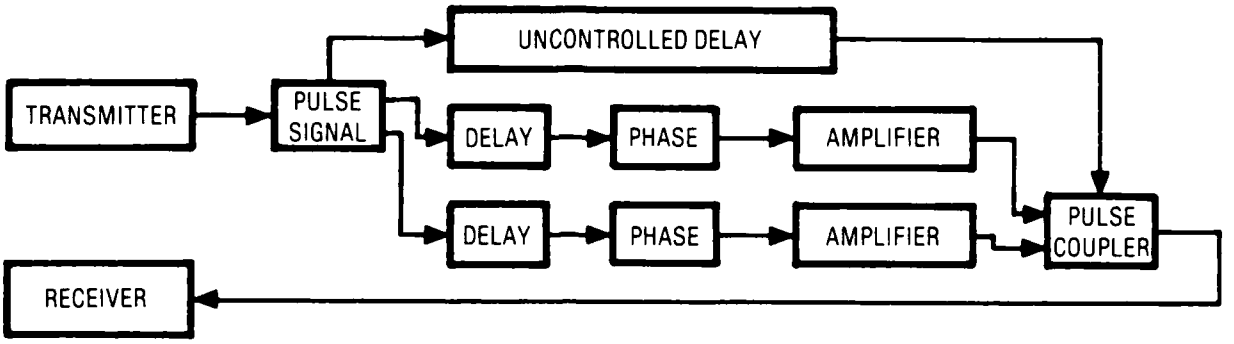


Figure 10. Block Diagram of 2-on-1 Null

In this 2-on-1 method, the delays are not matched. Instead, they are set to bracket the uncontrolled pulse. This relationship is shown in Figure 11 (τ might equal 4 ns).

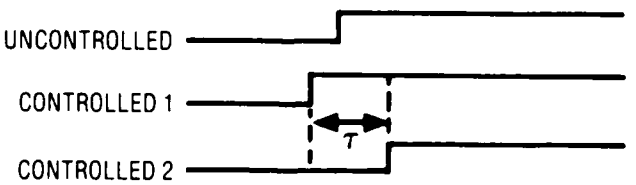


Figure 11. Uncontrolled Pulse Bracketing Relationship

The value of τ is set to produce the wanted bandwidth of null. The equation relating null bandwidth to τ is BW $\cong 0.4/\tau_2$ for a 20-dB null.

The 2-on-1 strategy is illustrated, in the phase domain, in Figure 12.

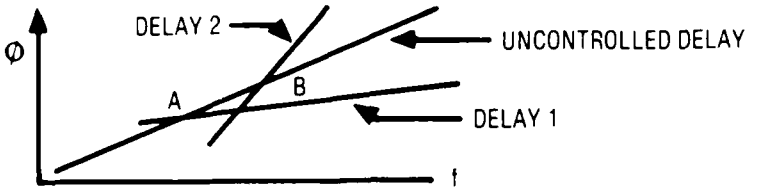


Figure 12. 2-on-1 Strategy in Phase Domain

The intersections (A and B) represent null points. The combination of two phase slopes produces a characteristic of a different slope. Figure 13 illustrates the phase slopes of two delay lines.

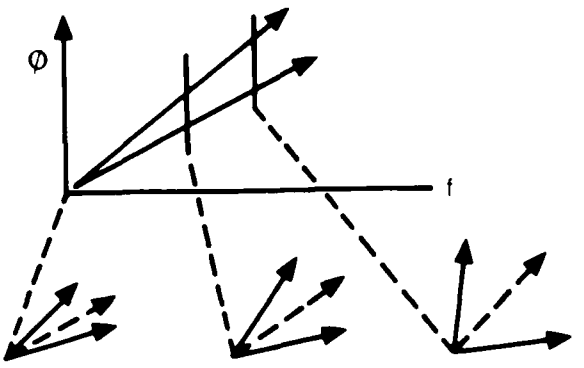


Figure 13. Phase Slopes of Two Delay Lines

At three points on two phase slopes, vector diagrams represent the phase relationship of each curve and the resultants. It is apparent that the resultant slope is intermediate between the two original slopes. With reference to Figure 12, the two controlled delay slopes add to match the uncontrolled delay slope from A to B and beyond.

FREQUENCY DOMAIN ILLUSTRATION OF 2-ON-1 STRATEGY

The frequency domain representation of a 2-on-1 strategy can be viewed as two pairs of delays. On pair is made from the uncontrolled path plus delay 1; the other is an uncontrolled path plus delay 2. The amplitude/frequency plots are shown as Figures 14 and 15. The cusps A and B are related to crossing points A and B in Figure 12.

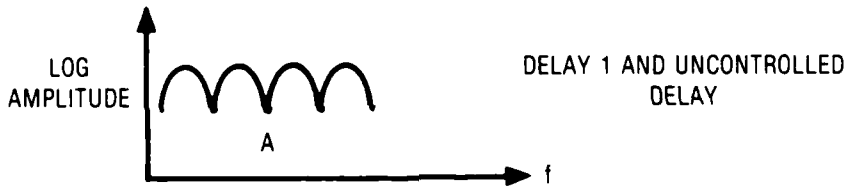


Figure 14. Amplitude/Frequency Plot of Path Pulse Delay 1

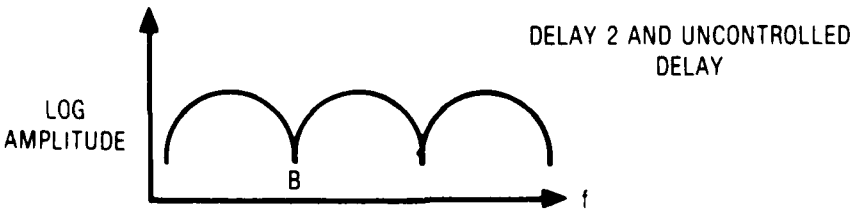


Figure 15. Amplitude/Frequency Plot of Path Pulse Delay 2

The cusps can be controlled by changing phase, as shown in Figure 16.

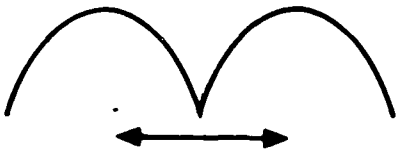


Figure 16. Cusp Control by Changing Phase

The cusps shown in Figure 14 and 15 can be moved in frequency so that they are coincident as shown in Figure 17.

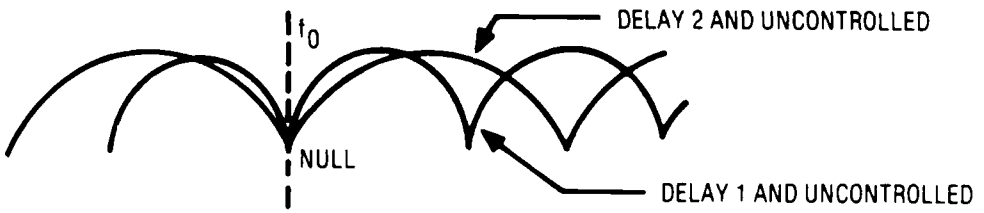


Figure 17. Coincident Cusps

CHANNEL DELAYS IN THE TIME DOMAIN

A reflecting surface with steps in range will produce delayed pulses with steps in time. A reflected pulse with multiple delays would have a form as shown in Figure 18.

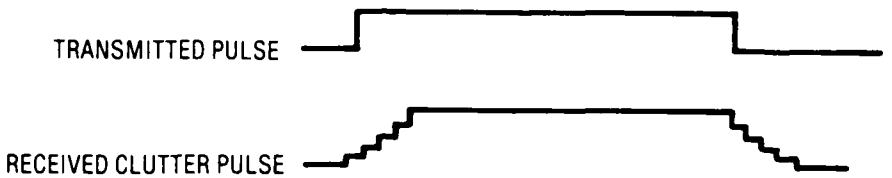


Figure 18. Form of Reflected Pulse with Multiple Delays

If the transmitted pulse were delayed to match the received pulse with a single delay, the difference between the pulses would contain "dog ears". Figure 19 shows this relationship. The step time of the resultant video waveform might be in the order of 4 ns.

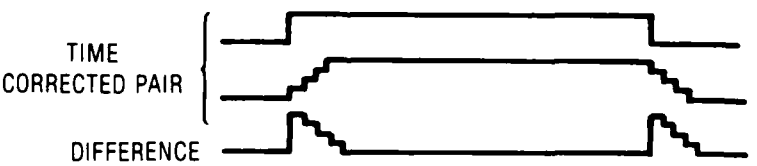


Figure 19. Relationship of Transmitted Pulse Delay Versus Received Pulse Delay

These dog ears will degrade the null somewhat, and might produce unwanted spikes, depending on the system bandwidth.

The ideal time relationship between reflected and feed-back signal is shown in Figure 20. The stairsteps are equal and a good video null is formed.

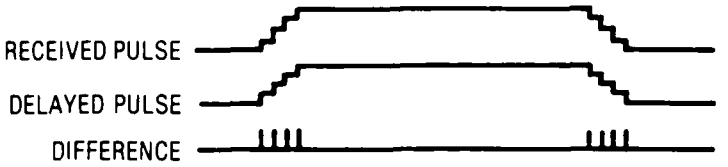


Figure 20. Ideal Time Relationship Between Reflected and Feed-Back Signal

As discussed in reference 1, stairsteps can be expressed by bandwidth limiting the receiver process to satisfy the Nyquist criteria for a given multiple delay spacing.

SECTION 3.
TEST SYSTEM DESCRIPTION

Figure A of Appendix A describes the overall three-port DRFM logic circuitry in block diagram form. The test configurations described in this section are essentially subsets of the overall DRFM in steps of increasing complexity, allowing for test and fine-trim adjustment at each stage of integration. The two DRFM delay channels are connected as a one-channel canceller (shown in Figure 21).

A 1 GHz $\pm$ 250 MHz signal is down converted to base band (I and Q channels). These two signals are biased to the required DC level, and are fed to delay channels. Each delay channel (a shift register) samples the signal and delays it by 1 to 7 clock cycles. The delayed output is selected by a digital multiplexer and is sent to an up converter. A conversion from 1 to 10 GHz is made. The up converter input is filtered to eliminate harmonics.

Each up converter output drives an attenuator and phase shifter. Each of the channels drives a power combiner. This power combiner simulates a system receiver. It has other inputs which will be discussed later.

The function of this two-channel circuit is to control gain, phase, and delay and to sum these signals.

A two-channel look-through block diagram is shown as Figure 22. This configuration has two controlled delay channels in combination with the DRFM and two uncontrolled cable delays. The DRFM and cable delays simulate a transmitter with reflections. The output power combiner, which simulates the system receiver input, receives signals from the cable delays and from the two cancellation paths. The sum of the cable delays (reflections) and the controlled delays should produce a null. When the wanted signal is combined with the four nulled channels, it should pass to the output of the power combiner.

Test equipment is connected to the canceller as shown in Figure 23. This circuit allows simulated input signal control and performance monitoring.

The 10-GHz signal generator is pulse modulated by the pulse generator by an RF switch. This signal is filtered to eliminate switch drive transients. The modulated signal is used to drive the canceller (either the configuration in Figure 21 or that in Figure 22). The canceller output is amplified and fed to time domain or frequency domain measurement instruments. This signal is amplitude detected by the crystal video receiver (CVR) and is displayed on the oscilloscope. A diode detector was sometimes used in place of the CVR when high speed was required. The spectrum analyzer, equipped with a scanning preselector, was used to monitor the frequency domain. The bandwidth of the signal is limited to 30 MHz in the preselector.

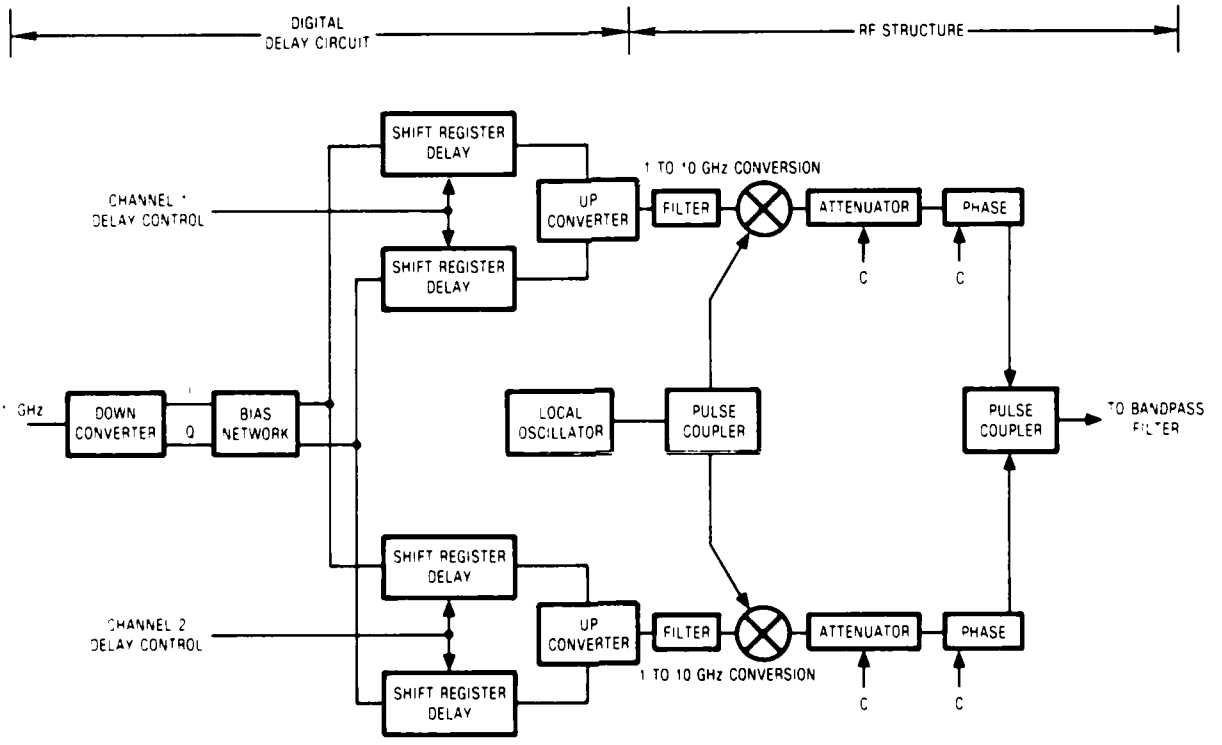


Figure 21. One-Channel Canceller

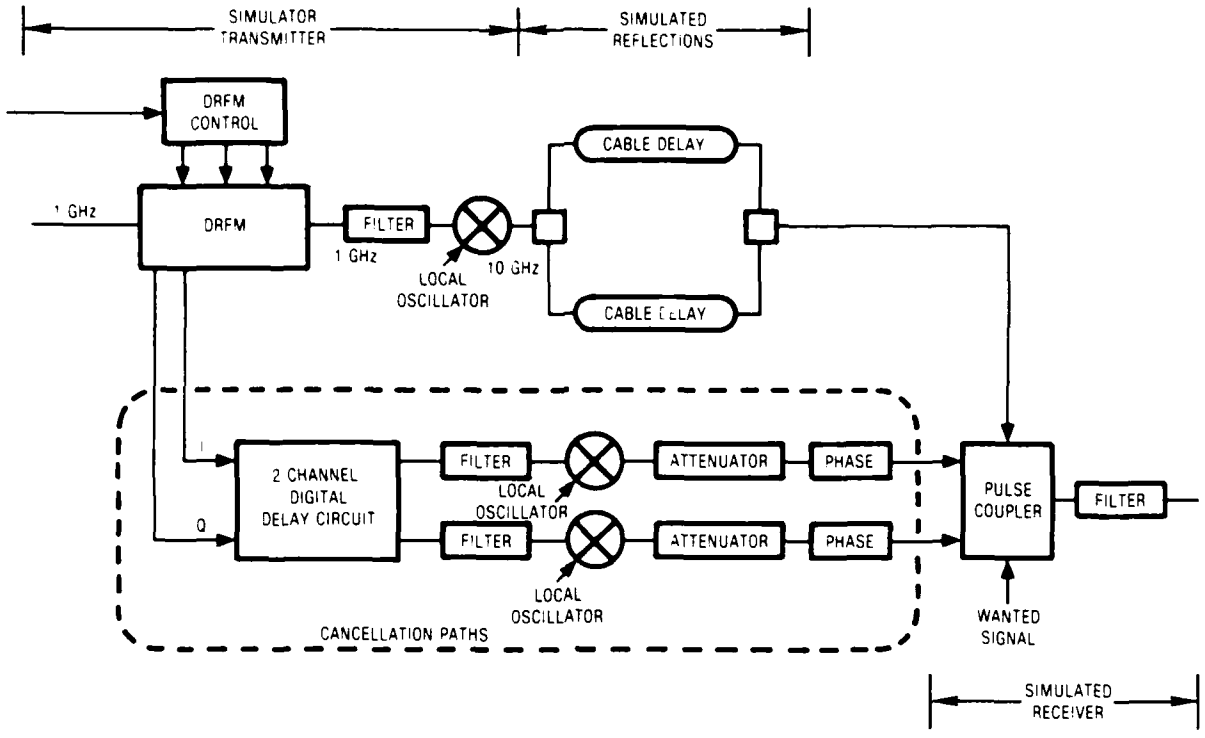


Figure 22. Two-Channel Look-Through Configuration

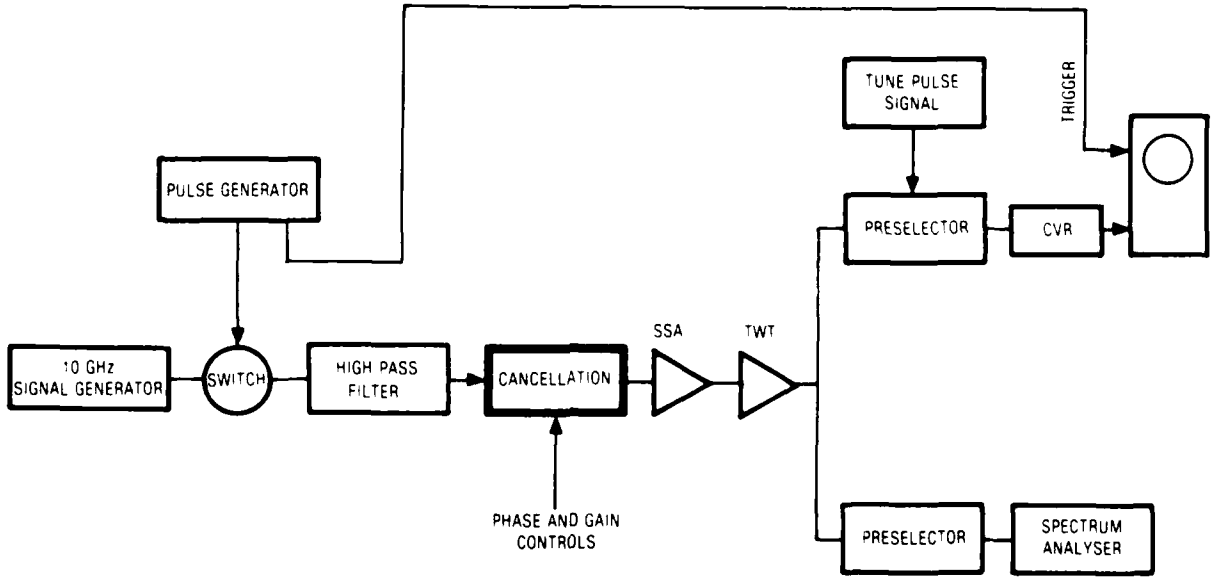


Figure 23. Test Setup

SECTION 4.
TEST SEQUENCE DESCRIPTION

This section will outline three groups of tests each having parametric variation. The test name is listed below and discussed in greater detail throughout this section.

a. 1-on-1 Tests
b. 2-on-1 Tests
c. 2-on-2 Test

1-ON-1 STRATEGY

In the 1-on-1 tests, gain, phase, and delay are adjusted to high accuracy to match amplitude, phase and phase slope of two channels using the configuration of Figure 21.

The first 1-on-1 test consists of digital delay circuit driving two analog microwave channels (continuous wave [CW] input). The purpose of this test is to establish the quality of nulls available with the test circuits that will support all other tests. In this test, delay 1 will be driven by a signal generator. The sampled input signal will be split into two signals which will drive the microwave nulling structure. This circuit assures that the two signals to be nulled are identical. It also assures that the two nulling channels are operating with typical noise and spur levels.

Digital delay 1 nulling digital delay 2 (CW input) is the second 1-on-1 test. This test nulls a common CW signal sampled by two different but "identical" circuits. This test is included to point out the difference between identical circuits.

Digital delay 1 nulling digital delay 2 with a pulse input is the third 1-on-1 test. This test is included to show the differences between CW and pulse nulling. It is also included to simulate future pulse system operation.

Digital delay 1 nulling digital delay 2 is the final 1-on-1 test. This test is included to demonstrate wide-band nulling of correlated system noise.

2-ON-1 STRATEGY

In these tests two digital delays are summed with an uncontrolled (reflected) delay channel using the configuration of Figure 22, with only one cable delay. The uncontrolled delay is generated by adding a cable delay to the DRFM output. The DRFM also drives the two digital delay channels. Phase and gain are adjusted accurately while digital delay is set to lead and lag the uncontrolled channel. The value of the digital delay is varied.

A 2-on-1 null with $\pm$ 3.5 ns (one shift register tap) delay and a 2-on-1 null with $\pm$ 7.0 ns (two shift register taps) delay are the tests utilized.

PARAMETRIC VARIATIONS ON 2-ON-2 STRATEGY

This test is an extension of the 1-on-1 strategy to two unequal, uncontrolled delays using the configuration of Figure 22. A 1-on-1 null is produced on each of two uncontrolled delays. Each null requires accurate adjustment of phase, gain, and delay. The difference in delay between uncontrolled channels is varied. The phase of the controlled channels is set to produce nulls at the same frequency, and is set to produce frequency offset nulls. The offset null approach is similar to "stagger tuning".

A 2-on-2 null with 13.0 ns reflection delay difference and common channel null frequency, a 2-on-2 null with 13.0 ns reflection delay difference and offset null frequencies, and a 2-on-2 null with 7.5 ns reflection delay difference and offset null frequencies are the approaches used for parametric variations on 2-on-2 strategy.

SECTION 5.
TEST RESULTS

The test results are presented in tabular form and in photographs. The following table gives Test Strategy, which describes the general test setup, Null Bandwidth achieved, and the Figure Number which describes the measured spectrum. The Test Descriptions are given in Section 4.

TEST STRATEGY	NULL BANDWIDTH	FIGURE NUMBER
1-on-1 CW	60 MHz	24
1-on-1 CW	80 MHz	25
1-on-1 Pulse		26
1-on-1 Spot Noise	Noise Bandwidth	27
2-on-1 Pulse	40 MHz	28
2-on-1 Pulse	60 MHz	29
2-on-2 13.0 ns	25 MHz	30
2-on-2 13.0 ns	See Figure	31
2-on-2 7.5 ns	35 MHz	32

RESULTS DISCUSSION

In general, the results table shows a decrease in null bandwidth from the simple first test to the more complex last test. One reason is that the more complex the circuit, the greater the chance for poor phase linearity.

CONTROL AND MISCELLANEOUS TESTS

The noise cancelling 1-on-1 test (Figure 27) produced the expected good null quality. Nosie is rejected by at least 20 dB over the bandwidth of the noise (about 30 MHz).

The pulse 1-on-1 test (Figure 26) was with two simultaneous pulses. The receiver signal pulse was passed while the unwanted reflection pulse was reduced by at least 20 dB. The unwanted pulse spectrum was rejected, since it was in the null bandwidth.

Spur reduction is shown in the spur cancelling 1-on-1 case in Figure 25. This pair of photos indicates a general reduction in spur amplitude in the cancelled bandwidth. If a particular spur were selected for cancellation, good results may be expected; however, with the reduction of one spur, one can expect an increase in another spur amplitude.

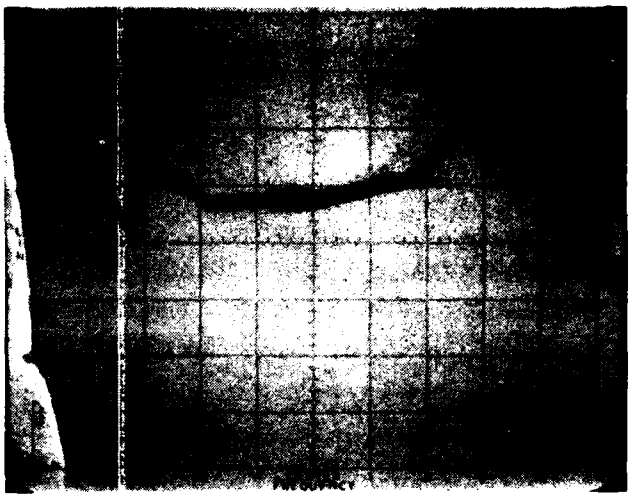
A control experiment involved driving the two RF channels with a signal generator. A 500-MHz bandwidth was obtained.

NULL EXPERIMENTS

For the 2-on-1 strategy, nulls of 40 and 60 MHz were measured and are shown in Figures 28 and 29.

For the 2-on-2 strategy, nulls of 25 to 35 MHz were measured. See Figures 30, 31, and 32. Nulls of 60 MHz were expected. To explain the discrepancy, a look at the hardware is required. Both delay channels were equipped with 270 degrees of phase shift control. The best null possible with this phase control limitation was obtained by changing delay so that phase control would produce a null. The result of this was to produce individual pair nulls of 30 MHz and 15 MHz. These nulls were combined to produce the 2-on-2 nulls presented in the results.

EQUIPMENT TEST - SAMPLED SIGNAL DRIVING RF STRUCTURE



SPECTRUM ANALYZER SETTINGS

VERTICAL = 10 dB/DIV

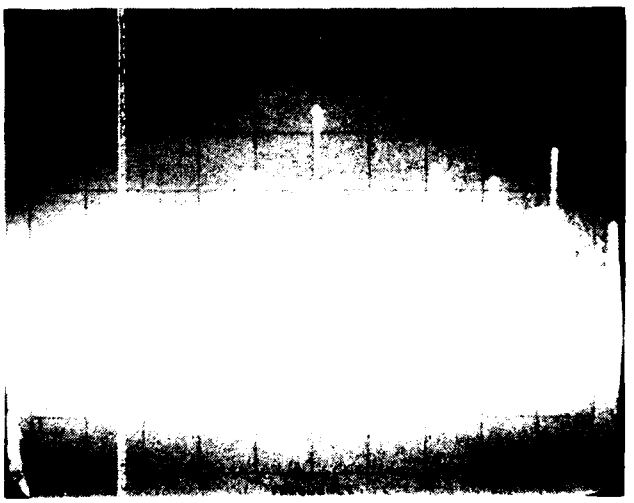
HORIZONTAL = 50 MHz/DIV

REFERENCE = -15 dB

NULL SPECTRUM

INPUT FREQUENCY ONLY

INPUT FREQUENCY SWEPT



SPECTRUM ANALYZER SETTINGS

(AS ABOVE)

ONE CHANNEL SPECTRUM (NOT NULLED)

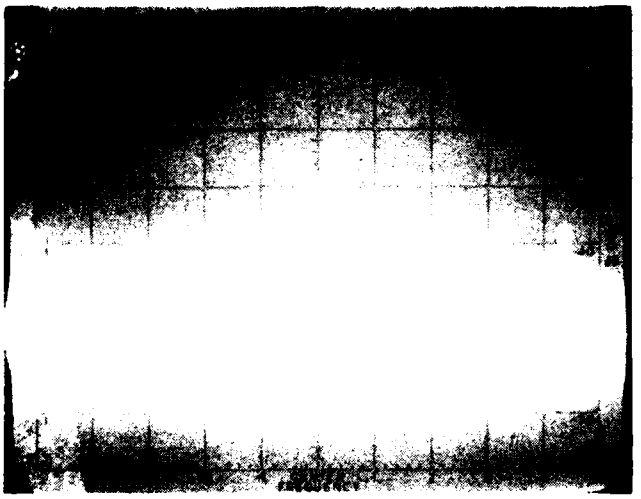
INPUT FREQUENCY SPURS

INPUT FREQUENCY STATIC AT fc

Figure 24. 1-on-1 CW at 60 MHz

EQUIPMENT TEST - SAMPLED SIGNAL DRIVING RF STRUCTURE

($\Delta T = 0$), CW



FREQUENCY ANALYZER SETTINGS

VERTICAL = 10 dB/DIV

HORIZONTAL = 50 MHz/DIV

REFERENCE = -10 dB

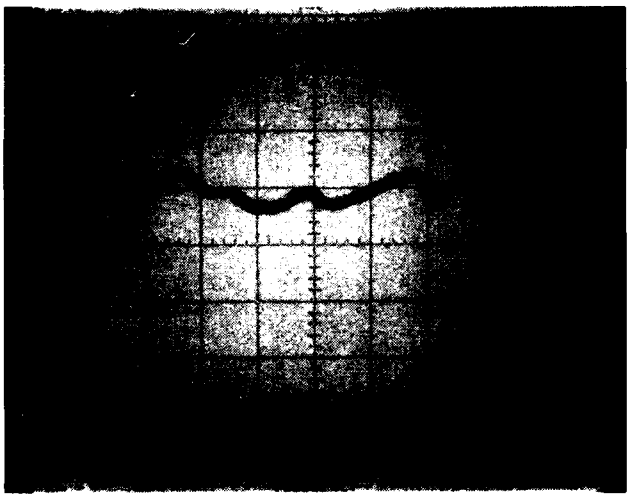
NULL SPECTRUM

INPUT FREQUENCY AND SPURS

INPUT FREQUENCY STATIC AT fc

Figure 24. 1-on-1 CW at 60 MHz (Cont.)

1-ON-1 NULL USING 2 DIGITAL DELAY CHANNELS



SPECTRUM ANALYZER SETTINGS

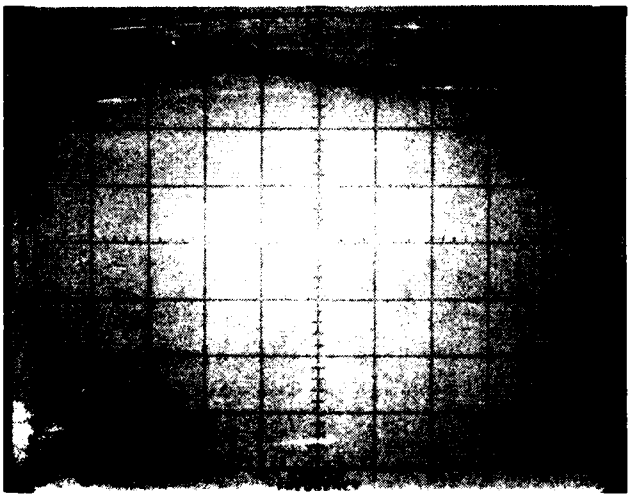
VERTICAL = 10 dB/DIV

HORIZONTAL = 10 MHz/DIV

CENTER

FREQUENCY = 10.58 GHz

DELAY = 0



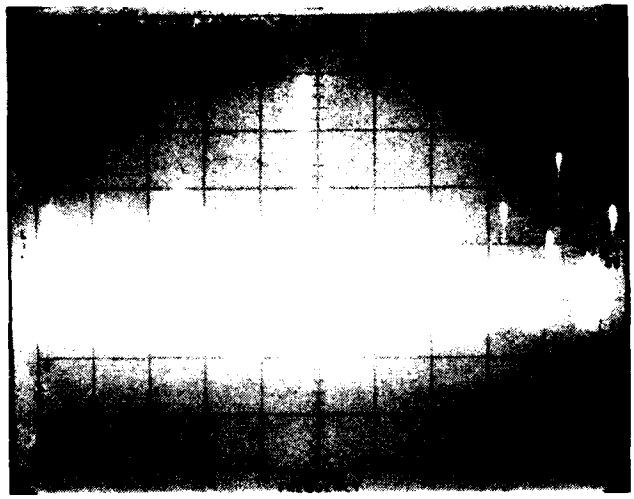
SPECTRUM ANALYZER SETTINGS

(AS ABOVE)

REFERENCE SPECTRUM

Figure 25. 1-on-1 CW at 80 MHz

SPUR NULLING 1-ON-1

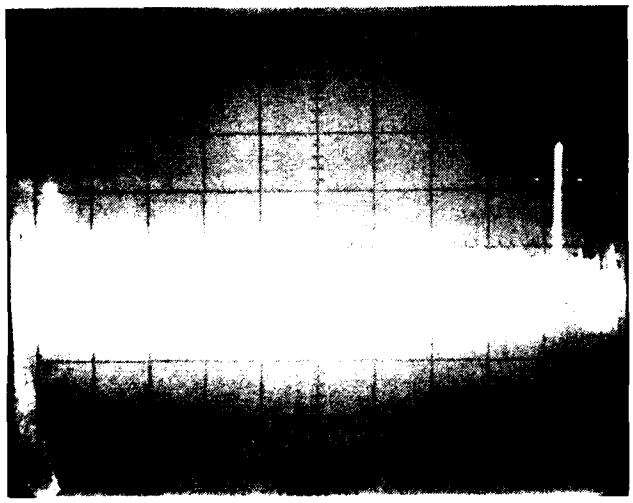


SPECTRUM ANALYZER SETTINGS

VERTICAL = 10 dB/DIV

HORIZONTAL = 10 MHz/DIV

DELAY 1 SIGNAL AND SPURS



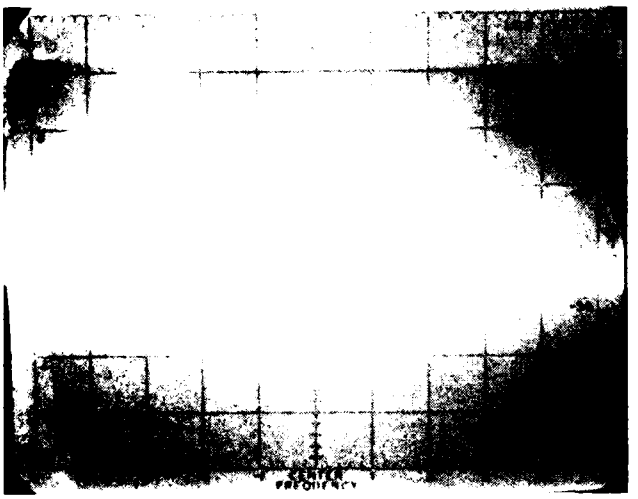
SPECTRUM ANALYZER SETTINGS

(AS ABOVE)

DELAY 1 NULLED AGAINST DELAY 2

Figure 25. 1-on-1 CW at 80 MHz (Cont.)

PULSE NULLING 1-ON-1



SPECTRUM ANALYZER SETTINGS

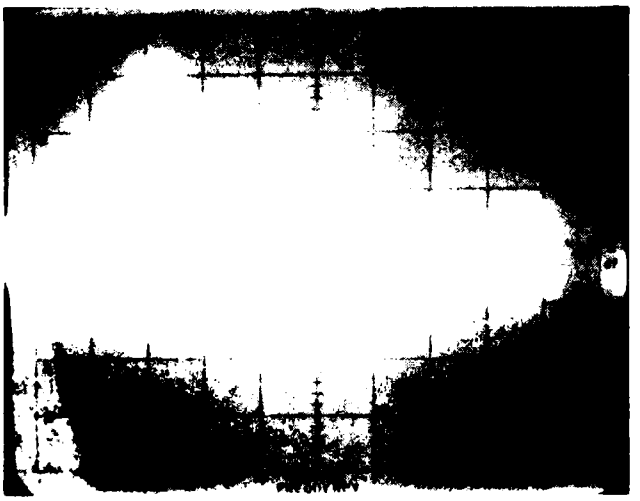
VERTICAL = 10 dB/DIV

HORIZONTAL = 2 MHz/DIV

FREQUENCY

SEPARATION = 9 MHz

BANDWIDTH = 300 kHz



SPECTRUM ANALYZER SETTINGS

(AS ABOVE)

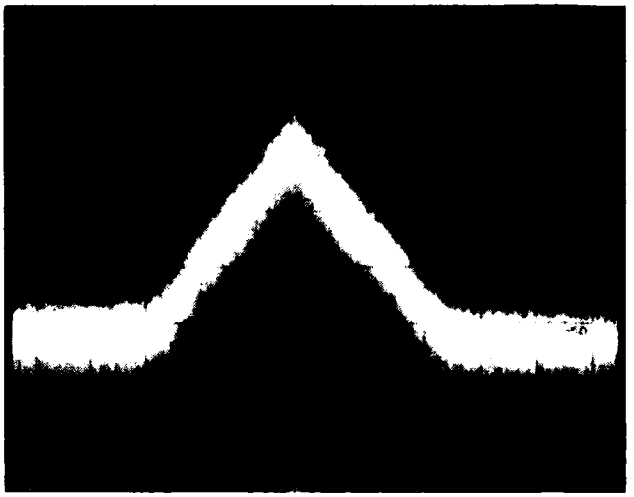
FREQUENCY

SEPARATION = 9 MHz

REFERENCE AND NULLED PULSE

Figure 26. 1-on-1 Pulse

1-ON-1 CANCELLATION (NOISE INPUT)

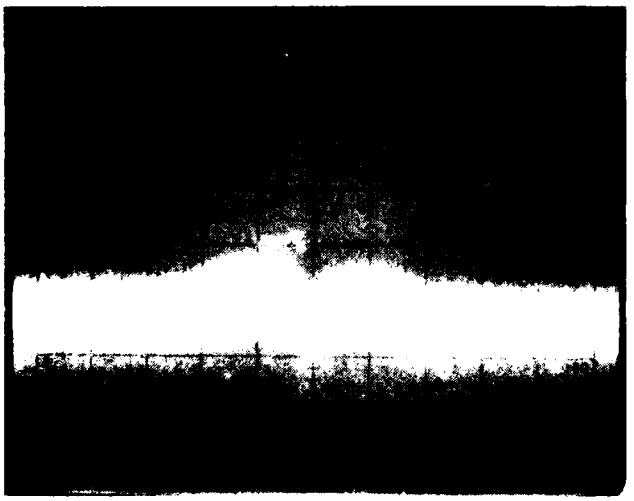


SPECTRUM ANALYZER SETTINGS

VERTICAL = 10 dB/DIV

HORIZONTAL = 10 MHz/DIV

ONE CHANNEL (UN-NULLED SPECTRUM)



SPECTRUM ANALYZER SETTINGS

(AS ABOVE)

NULLED SPECTRUM

Figure 27. 1-on-1 Spot Noise

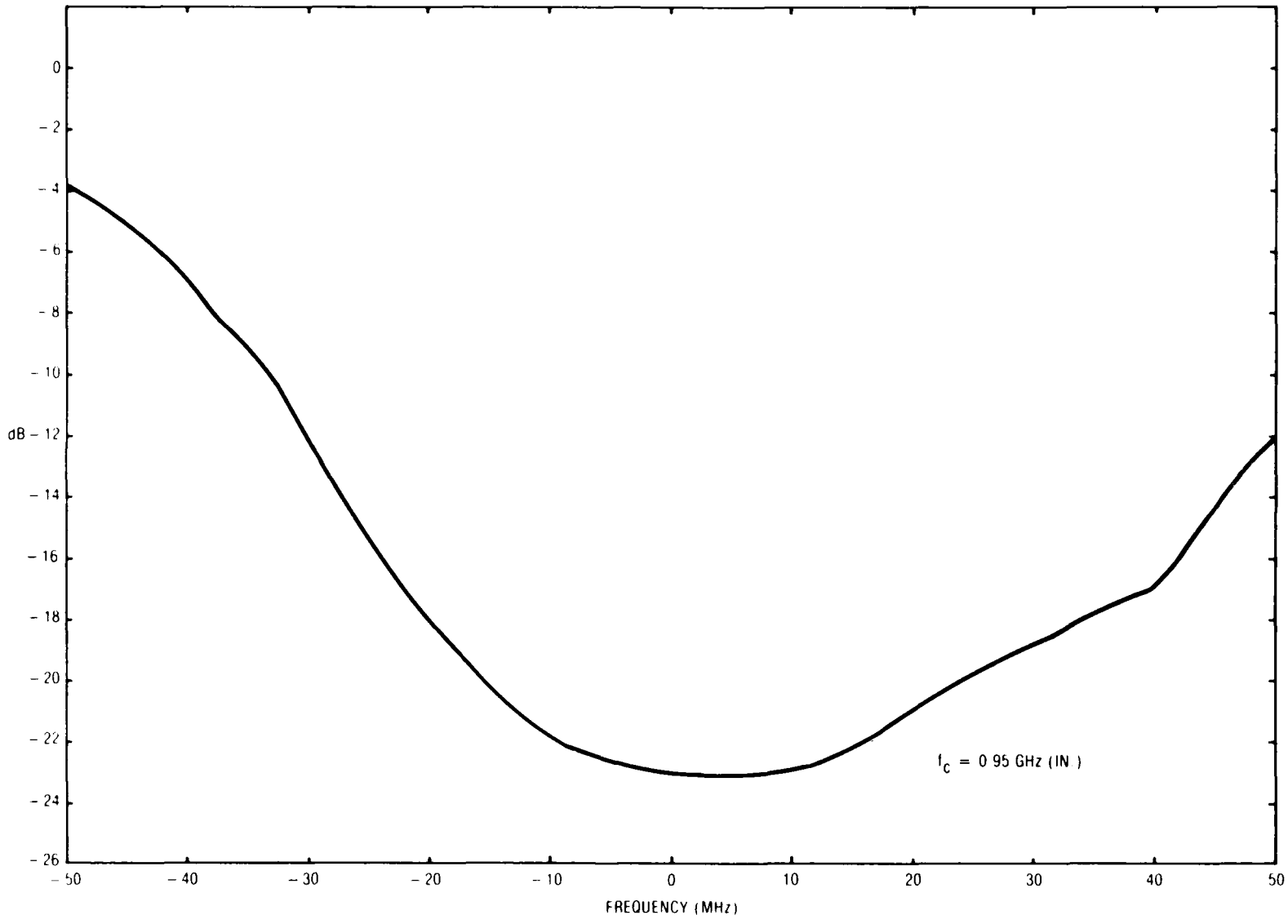


Figure 28. 2-on-1 Null With ± 3.5 ns Delay

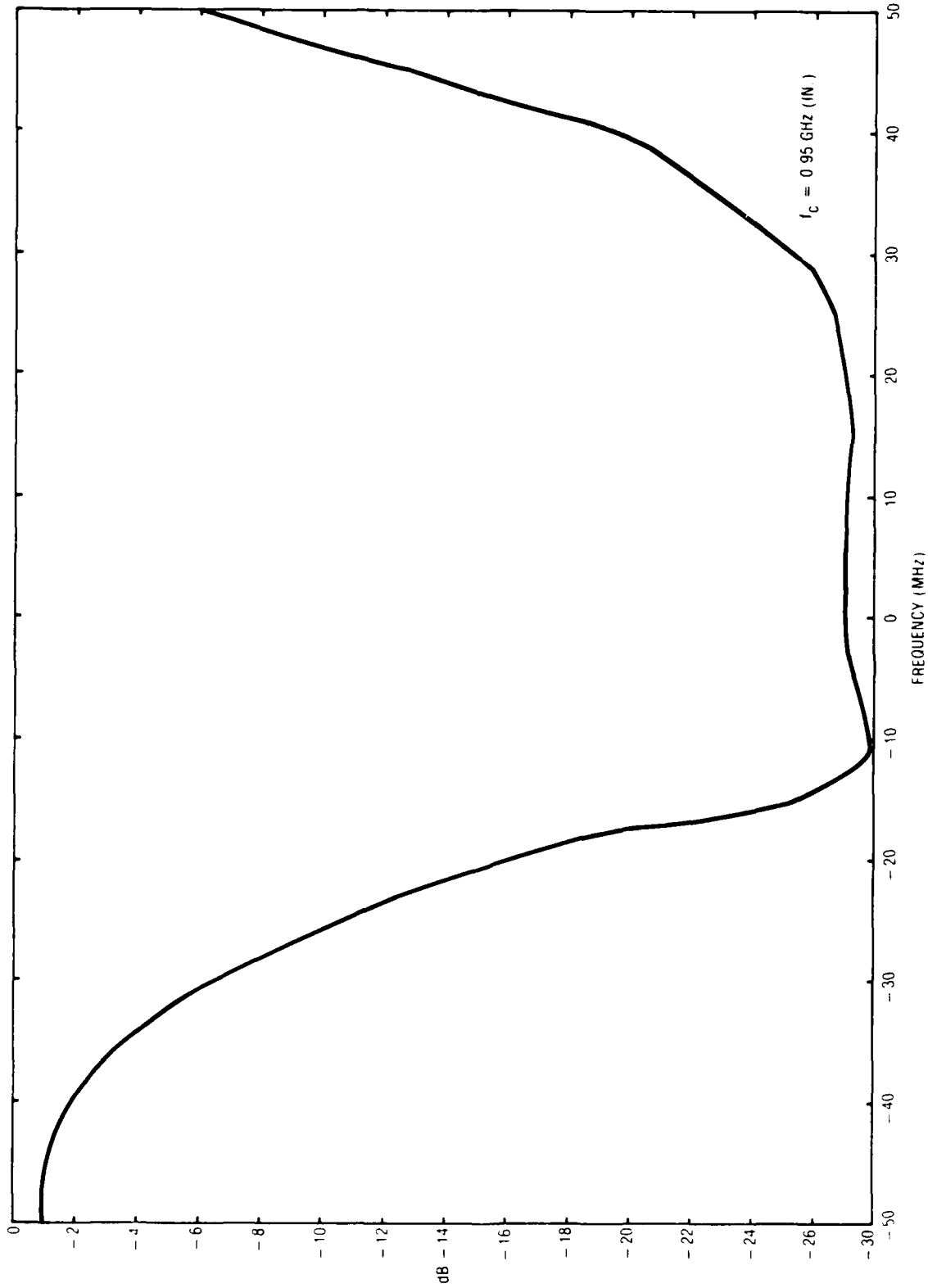


Figure 29. 2-on-1 Null With ± 7 ns Delay

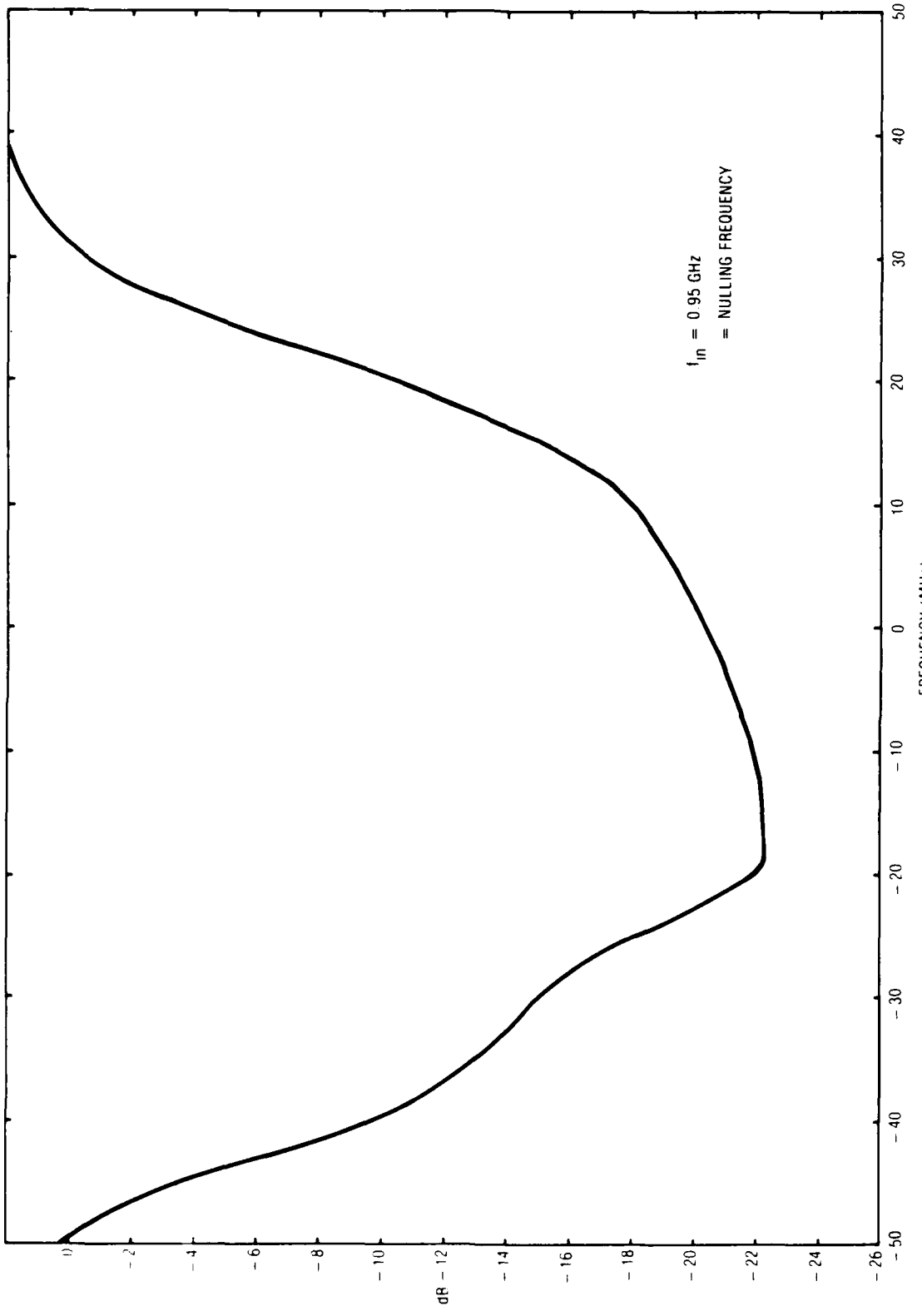


Figure 30. 2-on-2 Null With 13 ns Reflection Delay (Case 1)

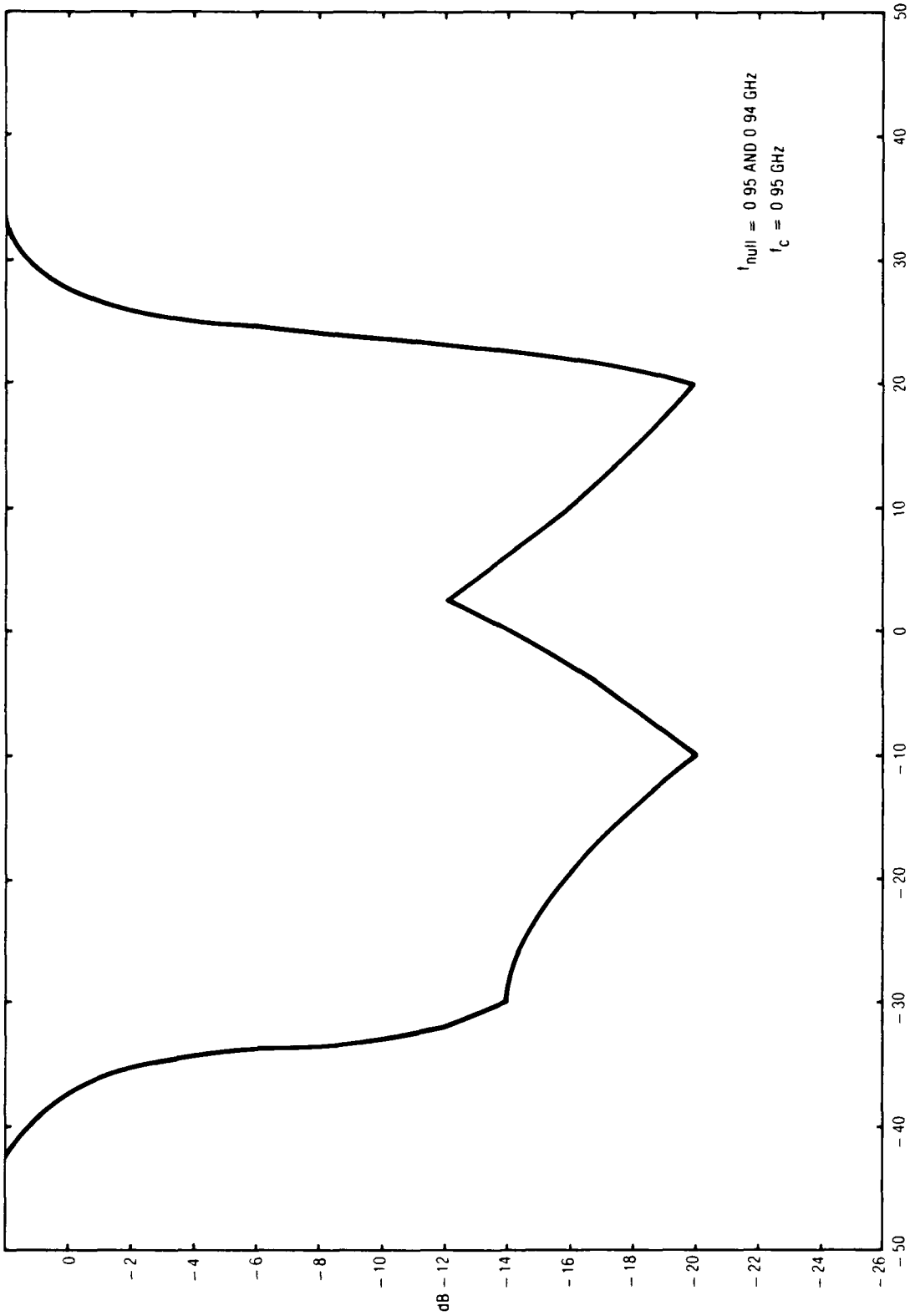


Figure 31. 2-on-2 Null With 13 ns Reflection Delay (Case 2)

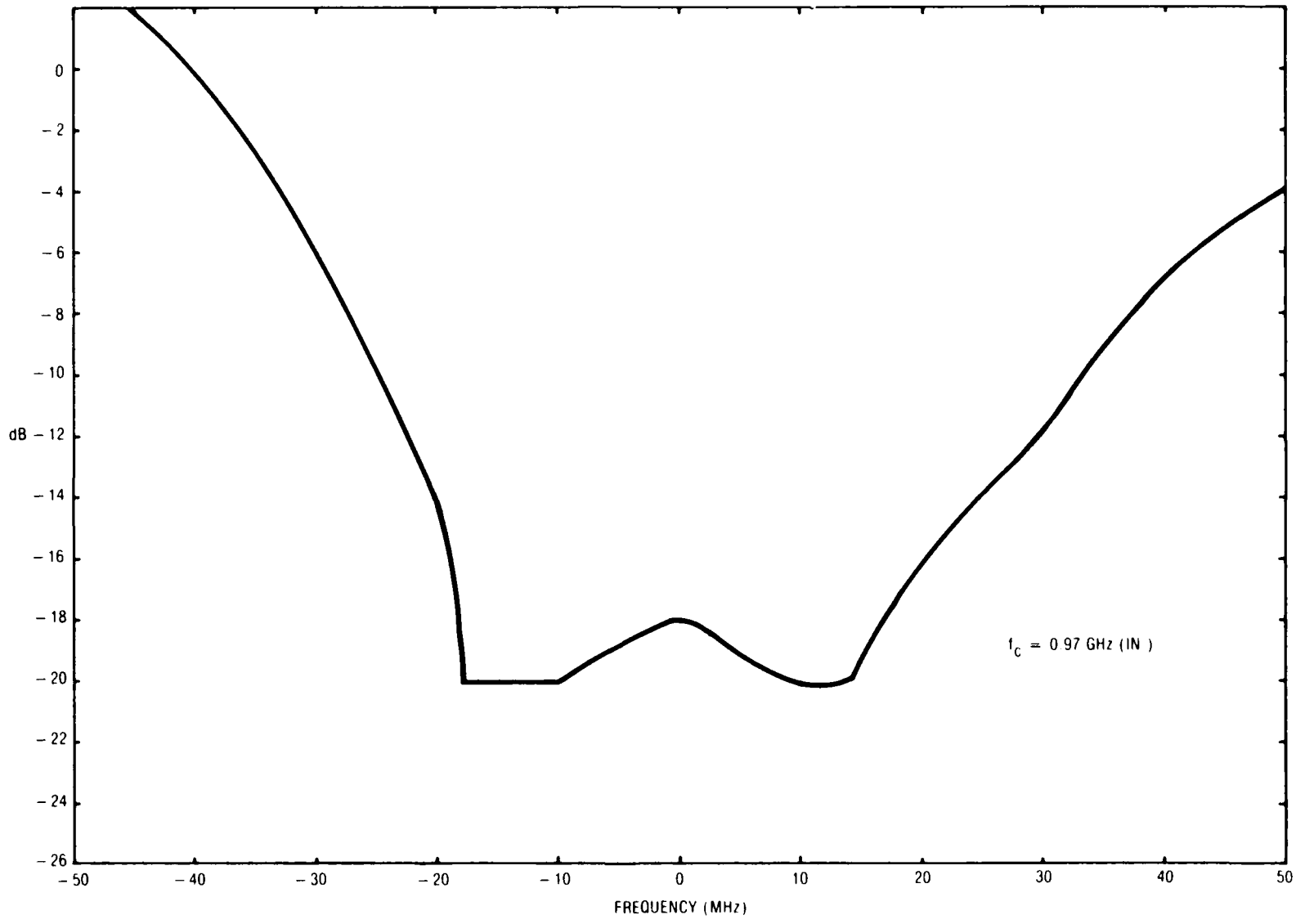


Figure 32. 2-on-2 Null With 7.5 ns Reflection Delay

SECTION 6.
CONCLUSIONS

The conclusions from the experiment are listed below in terms of Null Performance, Digital Delays, and Phase and Gain Adjustment Components.

NULL PERFORMANCE

1. Narrow band nulls of 45 dB are achievable.
2. Broad band (60 MHz) nulls of 20 dB are achievable.
3. Pulse, noise and CW null quality are comparable.

DIGITAL DELAYS

1. The circuits used suffered from high accuracy clock phasing requirements. Many points within the digital circuit required phasing to 5° accuracy.

2. The spur nulling was not good, which implies that some of the spurs were not controlled in phase. The matching of spur characteristics between two sampling circuits is not a practical process.

PHASE AND ADJUSTMENT COMPONENTS

Phase and gain adjustment components should be selected at variances of one parameter only. Phase shifters should have very little gain change and attenuators should have very little phase or delay change.

APPENDIX A

A.1 Circuit Description

The DRFM (digital section) is built with the following three blocks:

1. DRFM (15 μs memory length, 28 ns frame resolution)
2. Delay 1 (32 ns maximum memory length, 3.5 ns resolution)
3. Delay 2 (32 ns maximum memory length, 3.5 ns resolution)

Delay 1 and 2 are connected to the DRFM as shown in Figure A-1, the Digital Circuits Block Diagram. This block diagram shows the I and Q outputs of the DRFM coupled to the I and Q inputs of each of two delay circuits. This connection produces two variable output delays with respect to the DRFM output. Delay 1 and delay 2 are controlled independently to produce delays with a range of 28 ns at a resolution of 3.5 ns. Tapped duplex shift registers are used in the delay circuits.

The group of boards called delay 1 or 2 are modified DRFM boards which connect together with pins. The organization of the circuit boards is illustrated in Figure A-2. The physical unit is also shown in Figure A-2, with the left-most board in Figure A-2 corresponding to the top-most board in Figure A-2.

The shift register/mux board was a new design which was implemented on a DRFM sized board. The schematic is included as Figure A-3.

A.1.1 INTERFACE DESIGN

A.1.1.1 1-GHz Local Oscillator Distribution

Since each of the delay channels output through an up converter, a local oscillator signal is required. This signal originates in the DRFM.

A.1.1.1 1 GHz Local Oscillator Distribution (Cont.)

The circuit which amplifies and distributes the local oscillator signal is described in Figure A-4. The top half of the figure illustrates the original circuit. The bottom half shows the modification required. The changes include the addition of resistive power dividers and power amplifiers to provide sufficient power to the delay channels.

A.1.1.2 Clock Distribution

The original DRFM clock circuit is a crystal frequency multiplier circuit. The clock frequency is multiplied to produce the local oscillator frequency. In Figure A-5 (top), a portion of the tuned multiplier is shown driving a synchronized oscillator (U1-A). Figure A-5 (bottom) shows the modification to the original circuit allowing for the driving of three synchronized clock oscillators.

The emitter follower circuit (Q_A) drives a tuned auto transformer circuit to lower the impedance from 2000 ohms at (Q9) to 50 ohms. The 50-ohms signal drives two 402 amplifiers in series. The high level signal, thus formed, is split into three channels to drive the three synchronized clock oscillators. The bias resistors set U1-A, Pin 17 to the optimum voltage for oscillator operation. The oscillator power is split in U1-B and U1-C after being delayed. The delay is sufficient to put the local oscillator in phase at all frequency converters.

A.1.1.3 Output Blanking

The DRFM output blanking is driven with an internally generated emitter coupled logic signal. The function of the output blanking switch is to eliminate intra-pulse noise. The delay circuits were equipped with the output blanking switch, but no internally generated drive signal. To allow blanking from an external source, the blanking switch drive was modified to transistor-transistor logic levels . Figure A-6 (top) shows the original circuit, while Figure A-6 (bottom) illustrates the delay board circuit as modified.

A.1.1.3 Output Blanking (Cont.)

In future systems using the delay boards, further attention must be paid to correct blanking timing. The delay circuits generate noise between pulses of appreciable power. Clock feedthru is the major offender.

A.1.2 LESSON LEARNED FROM THE TEST HARDWARE

A.1.2.1 Control Cross Coupling

In general, the problems fell into the multiple adjustment category. Each channel required gain, phase, and delay adjustment. There was cross coupling between gain and delay controls; cross coupling between phase and gain controls; and phase balance effects due to digital circuit internal clock phasing. In all there were six cross coupled adjustments per channel.

A.1.2.2 Component Requirements

The bandwidth of the components in a nulling system must include the complete band of interest. The requirements of phase and gain flatness are extreme; five degrees and 0.1 dB are reasonable requirements over the band of interest. Depending on the system design, the band of interest might be 500 MHz (DRFM bandwidth) or 70 MHz (measured a null bandwidth).

A.1.2.3 DRFM Circuits

The design of the DRFM maximizes bandwidth in every detail. Any changes to the circuitry tend to reduce bandwidth, or increase spur level. Redesigning the clock distribution circuits was of particular detriment to DRFM performance. These circuits were optimized over less than the full 500 MHz. A 100 MHz full performance band was achieved. Outside of this band, spurs and gain slope were poorer than specification. The test results were not affected by this, since all test nulls were less than 100 MHz.

A.1.2.4 DRFM Mechanics Affected "Tune-Up"

The DRFM is built like a deck of cards connected with orthogonal interconnecting pins in order to achieve small size and short circuit paths. Circuit development required shuffling the cards to set up particular tests. As card positions changed, circuit capacity changed, and circuit operation was modified. As a result of these practical matters, modification and "tune-up" were very time consuming.

In many cases, pin-to-pin connections were not possible. Instead, coax connections were used to maintain impedance and to reduce pickup. The assembly, as completed, was not adaptable to the usual liquid cooling and was effectively substituted by air cooling. Changing the configuration of the boards caused some component failure. In addition, some chip bypass capacitors, when flexed, cracked. Capacitor failure changed system performance in subtle ways.

The lessons learned from the building and testing of the NAVELEX DRFM are:

1. The data presented is valid.
2. The hardware, as built, is limited in bandwidth and spur performance.
3. Basic modification of DRFM circuits is as time consuming as the original design.
4. With new requirements on the DRFM, new circuit approaches are indicated.

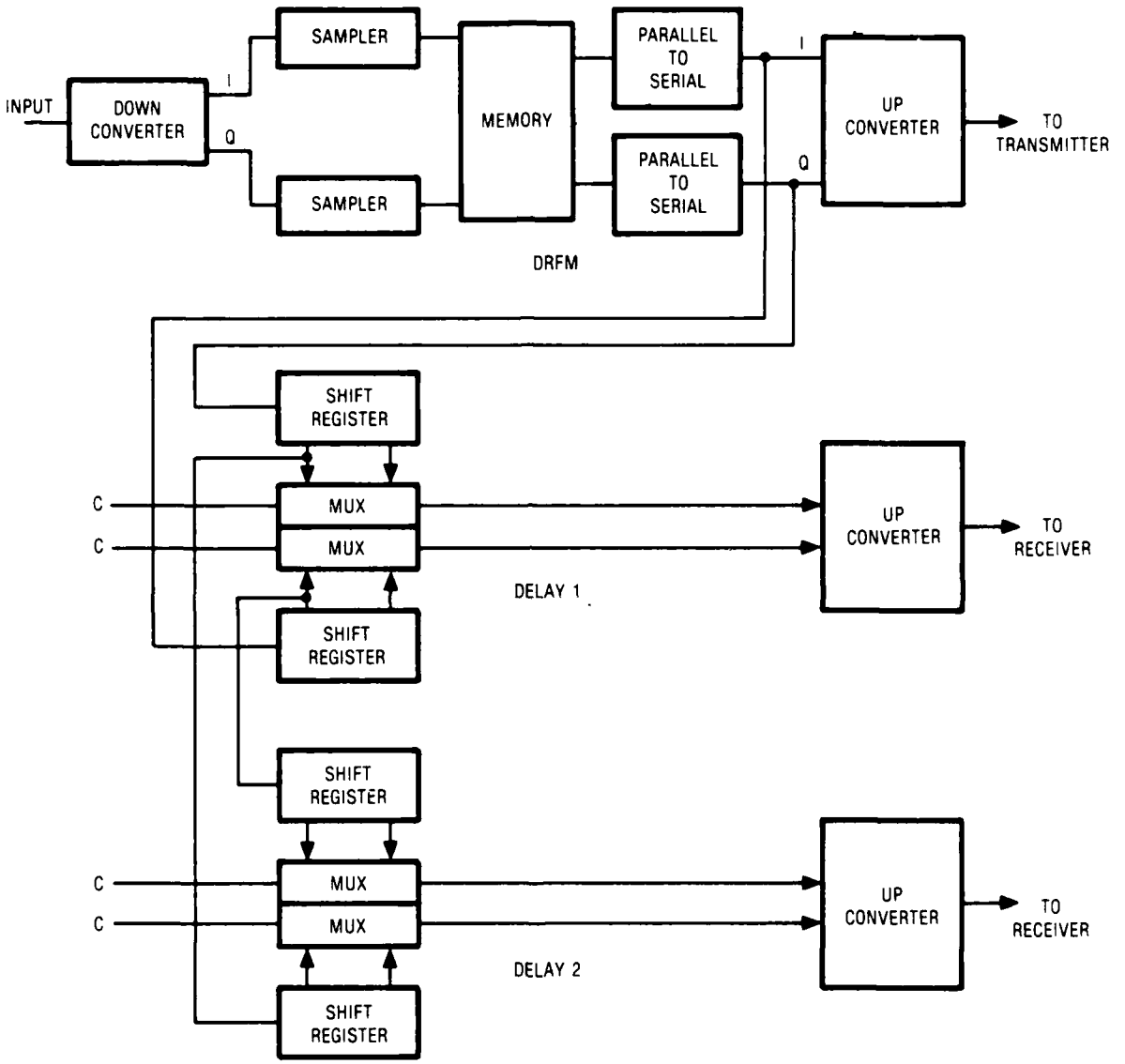


Figure A-1. Digital Circuits Block Diagram

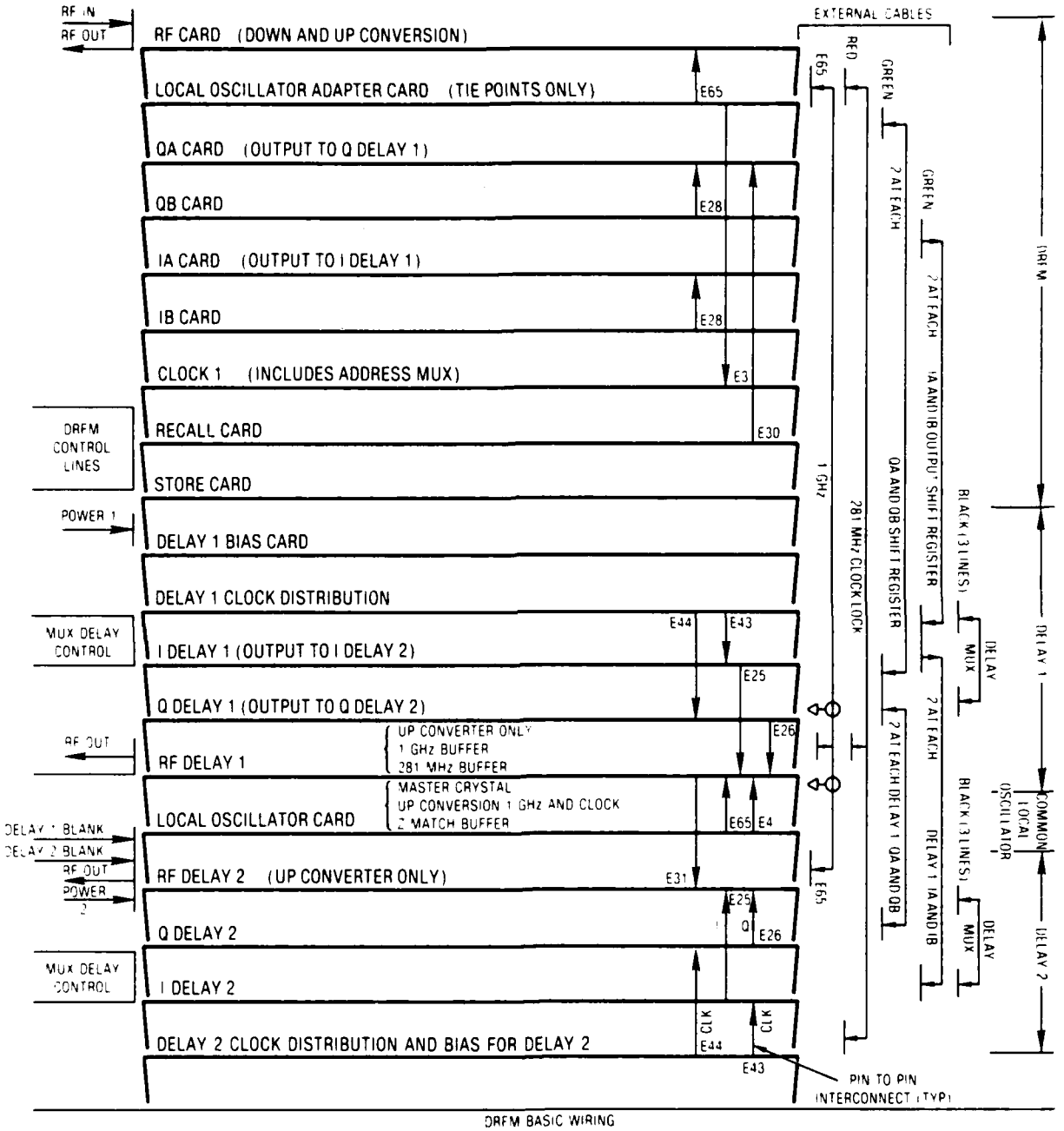


Figure A-2. Organization of Circuit Board Stack

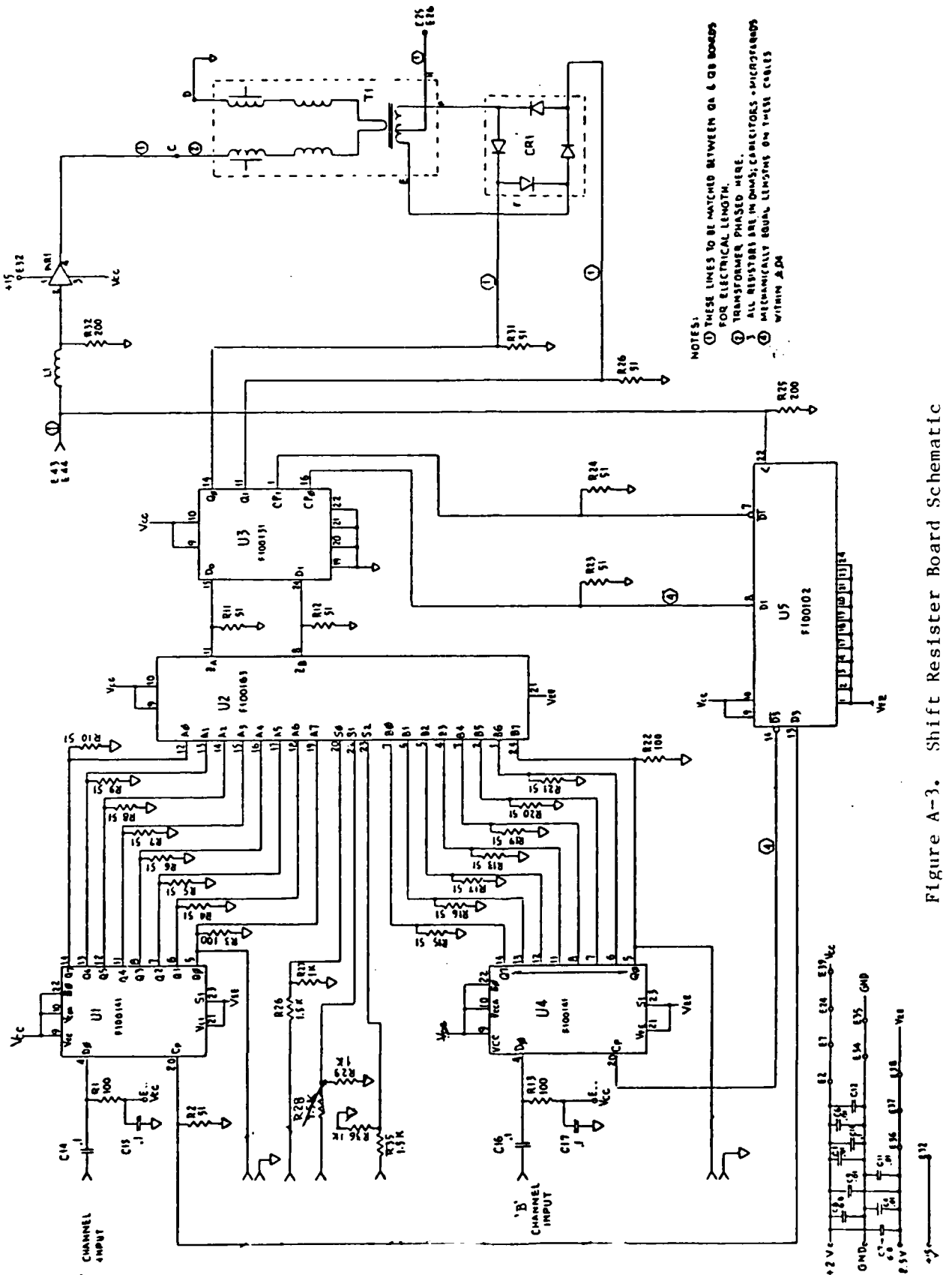


Figure A-3. Shift Resister Board Schematic

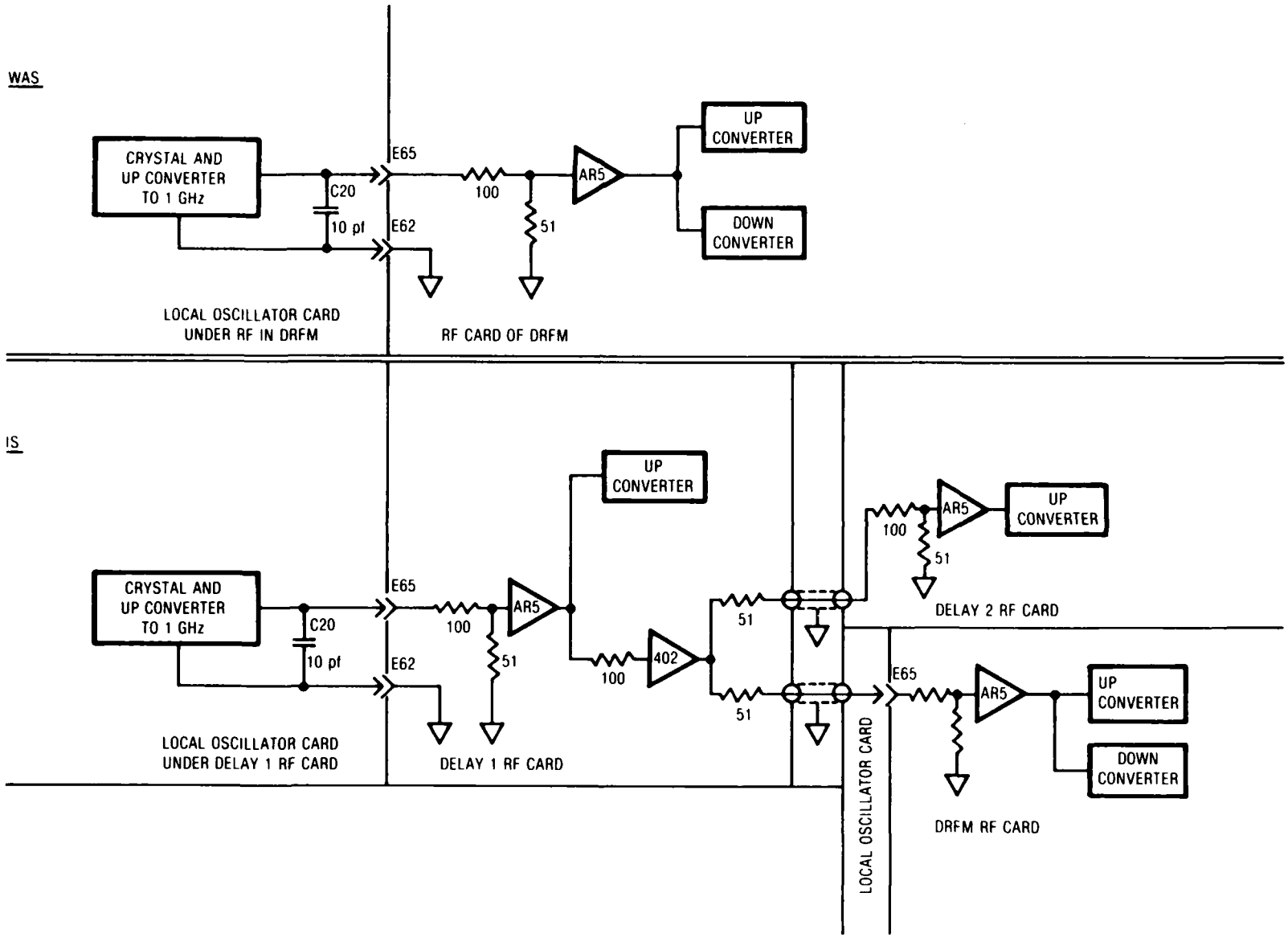


Figure A-4. Circuit Amplification and Distribution of the Local Oscillator

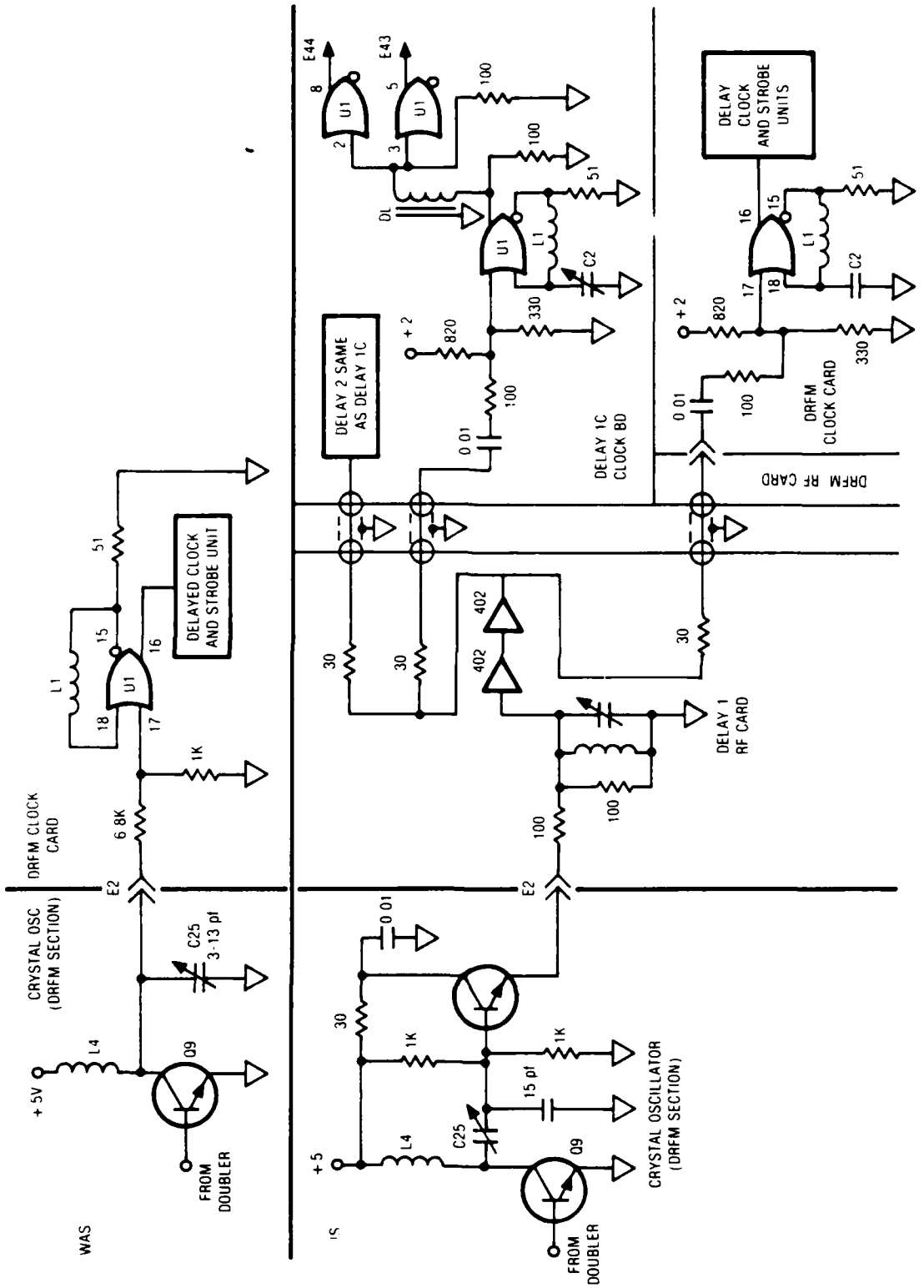


Figure A-5. Clock Distribution

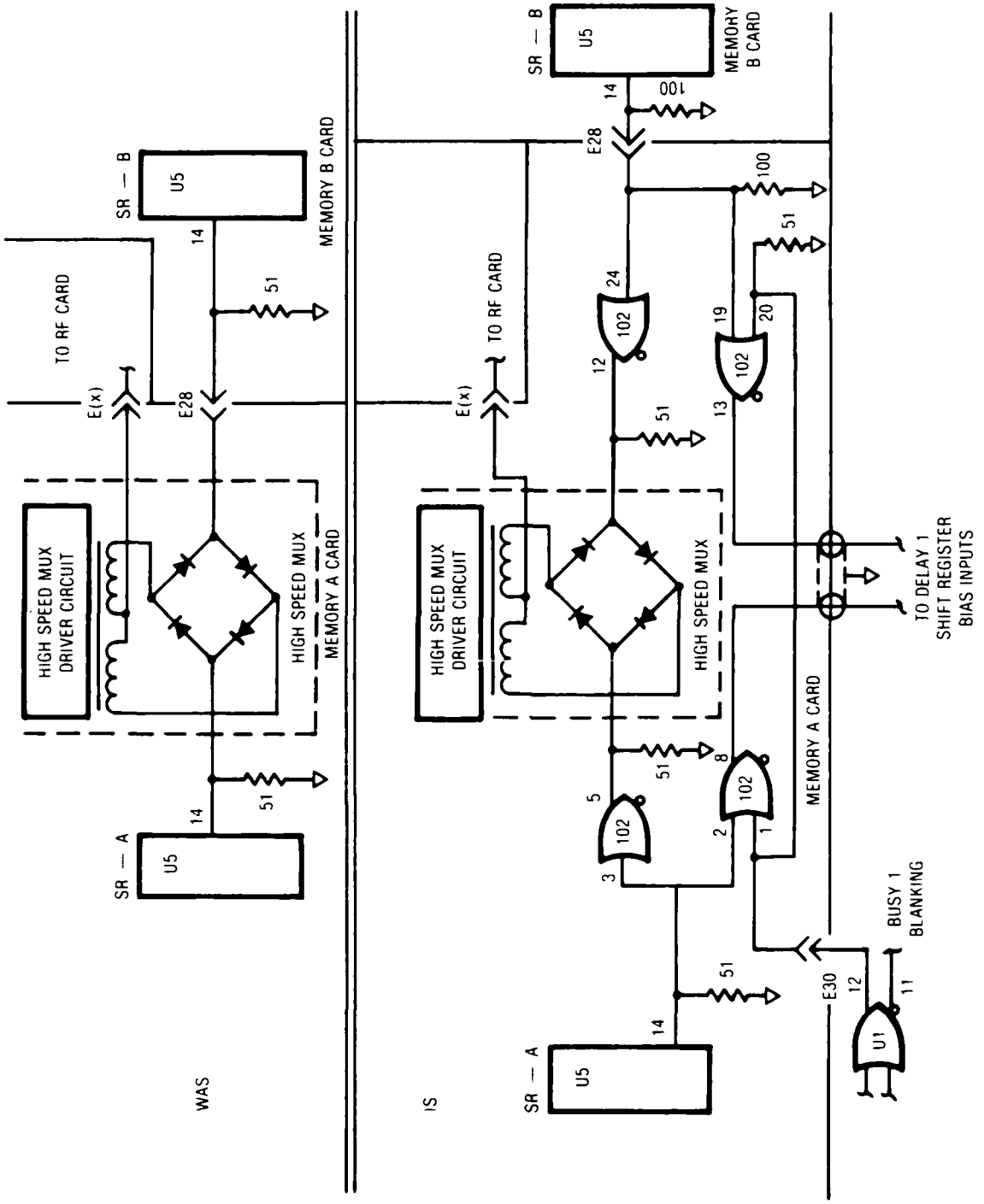


Figure A-6. Output Blanking

END

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